## Remarks

Clarifying amendments have been made to claims 1 and 14 to better define that which the Applicant considers to be the invention. The amendments do not add new matter. Claims 1-24 are pending.

## Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Riley et al. (U.S. Patent No. 6,266,731)("Riley") in view of Schwaderer (White paper, "Domain Validation Explained")("Schwaderer"). Further, the Examiner rejected claims 2-4, 18-21, 23 and 24 under Riley and Schwaderer in view of Kwan et al. (U.S. Patent No. 6,658,459)("Kwan"). As will be fully explained, the cited prior art references do not disclose or suggest each and every feature of independent claims 1, 14, and 21 as required to raise a prima facie case of section 103 obviousness.

Applicant respectfully submits that a prima facie case of obviousness must include the disclosure or suggestion of every feature of the claimed invention. Applicant submits that each and every feature of the claimed invention is not disclosed or suggested by the cited prior art references.

Applicant respectfully submits that at the very least Riley does not disclose or suggest the generating a key data pattern. As defined by the specification, the key data pattern includes information about an initiator and the host. The Office is directed to column 12, lines 36-40 of Riley (which the Office itself has cited in the final Office Action) which states:

> Each transaction includes the identity of the initiator (Initiator Number), the initiator's bus segment (Bus Number) and

> transaction sequence (or "thread") to which it belongs (Sequence Number).
>
> An extended command field further qualifies each transaction.

The cited portion above specifically states that each transaction includes: (1) the identity of the initiator, (2) the initiator's bus segment, (3) and transaction sequence. The cited portion of Riley does not disclose or suggest usage of both information regarding the host and the initiator. Consequently, Applicant respectfully submits that cited portions of Riley do not disclose or suggest that the key data pattern includes the identity of the initiator and the host.

Applicant further respectfully submits that Riley does not disclose or suggest the identification of the first initiator being included within the key header. In the cited portion of Riley shown above, Riley teaches that a transaction contains an identity of the initiator but does not indicate or suggest usage of a key header which includes the identity of the initiator.

Furthermore, the Applicant respectfully submits that, at the very least, the feature of examining the key data pattern to ascertain a level of communication integrity of a physical connection with the target to determine a throughput capability of the physical connection is not disclosed or suggested in the cited prior art references. The Office cites column 12 lines 36-40 of Riley and suggests that this feature is disclosed by the cited portion of Riley. Applicant respectfully traverses these suggestions. As used by Riley an extended command is used to qualify the type of transaction and attributes being used by the initiator. As defined in table 1 of Riley, the extended command is used for further qualification of the type of command the initiator is attempting. Therefore, Applicant respectfully submits that "qualifies" as used by Riley does not disclose or suggest the examining the key data pattern to ascertain a level of communication integrity of a physical connection to determine a

throughput capability of the physical connection. Applicant respectfully submits that the cited portions of Riley do not disclose or suggest this feature.

The Office further cites to column 12, lines 17-32 of Riley to support its assertion that Riley suggests verification of bus performance. This suggestion is also traversed. Column 12, lines 17-32 of Riley states as follows:

> A. Overview of Registered PCI
> According to the present invention, Registered PCI introduces several major enhancements to the PCI Specification as follows:
>
> 1. Higher clock frequencies such as, for example, 133 MHz.
> 2. Signaling protocol changes to enable registered outputs and inputs, that is, device outputs that are clocked directly out of a register and device inputs that are clocked directly into a register. Signal switching is generally restricted such that devices can signal 2 clocks before an expected response from other devices with the least impact to bus performance.
> 3. New information passed with each transaction that enables more efficient buffer management schemes.

As shown in the cited portion of Riley, Riley teaches that devices can signal 2 clocks before an expected response from other devices with the least impact to bus performance. Therefore, Applicant respectfully submits that the cited portion of Riley does not verify bus performance but merely advocates restricting signal switching so the impact to bus performance is minimal. Applicant respectfully submits that this is not actively verifying a throughput of a physical connection between an initiator and a target. Therefore, Applicant submits that the cited prior references do not disclose or suggest all features of the claimed invention.

The Office further suggests that ascertaining a level of communication integrity is inherent in Riley as shown by column 5, lines 35-43 of Riley. Applicant disagrees. Column 5, lines 35-43 states as follows:

> The present invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing in a computer system a registered

> peripheral component interconnect bus, logic circuits therefor and signal protocols thereof. In the present invention, hereinafter referenced as Registered PCI ("RegPCI"), all signals are sampled on the rising edge of the PCI bus clock and only the registered version of these signals are used inside the RegPCI devices.

Applicant submits that "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic," and "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See M.P.E.P. 2112 Applicants do not see any factual and/or technical reasoning to support the Office's assertion of inherency. The cited portion of Riley only discusses usage of registered PCI and usage of registered signals. Applicant submits that this is not a disclosure or suggestion that a level of communication be ascertained by examining the key data pattern to determine a throughput capability of the physical connection. Therefore, for at least the reasons discussed above, Applicant submits that the cited prior art references do not disclose or suggest all of the features of the independent claims 1, 14, and 21.

Moreover, Applicant respectfully submits that, at the very least, one skilled in the art would not combine the teachings of Riley and Schwaderer because Riley teaches device configuration and not bus performance verification. Therefore, combining Schwaderer with a reference that provides motivation for *device configuration* does not render obvious the claimed invention for *verifying bus performance*. Thus, the teachings of Riley would not motivate one of ordinary skill to combine the reference with Schwaderer to render Applicant's claimed invention obvious. Consequently, Applicant respectfully requests withdrawal of the 35 U.S.C. §

103(a) rejection. Applicant further submits that the claims depending directly or indirectly are allowable for the at least the same reason as the independent claims.

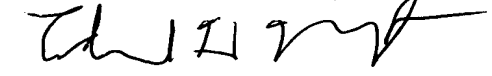
**Applicability of 35 U.S.C. 103(c)**

Applicant respectfully submits that Adaptec Inc. was the assignee of the Kwan reference at the time the claimed invention was made. The present application is also assigned to Adaptec, Inc. and was subject to an obligation of assignment to Adaptec, Inc. at the time the claimed invention was made. Therefore, under 35 U.S.C. 103(c), Applicant respectfully submits that the Kwan reference is disqualified. Consequently, Applicant respectfully submits that claims 2-13 and 15-24 are allowable.

Applicant further submits that the claims depending directly or indirectly are allowable for the at least the same reason as the independent claims.

Applicant respectfully requests a Notice of Allowance based on the foregoing remarks. If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP137). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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